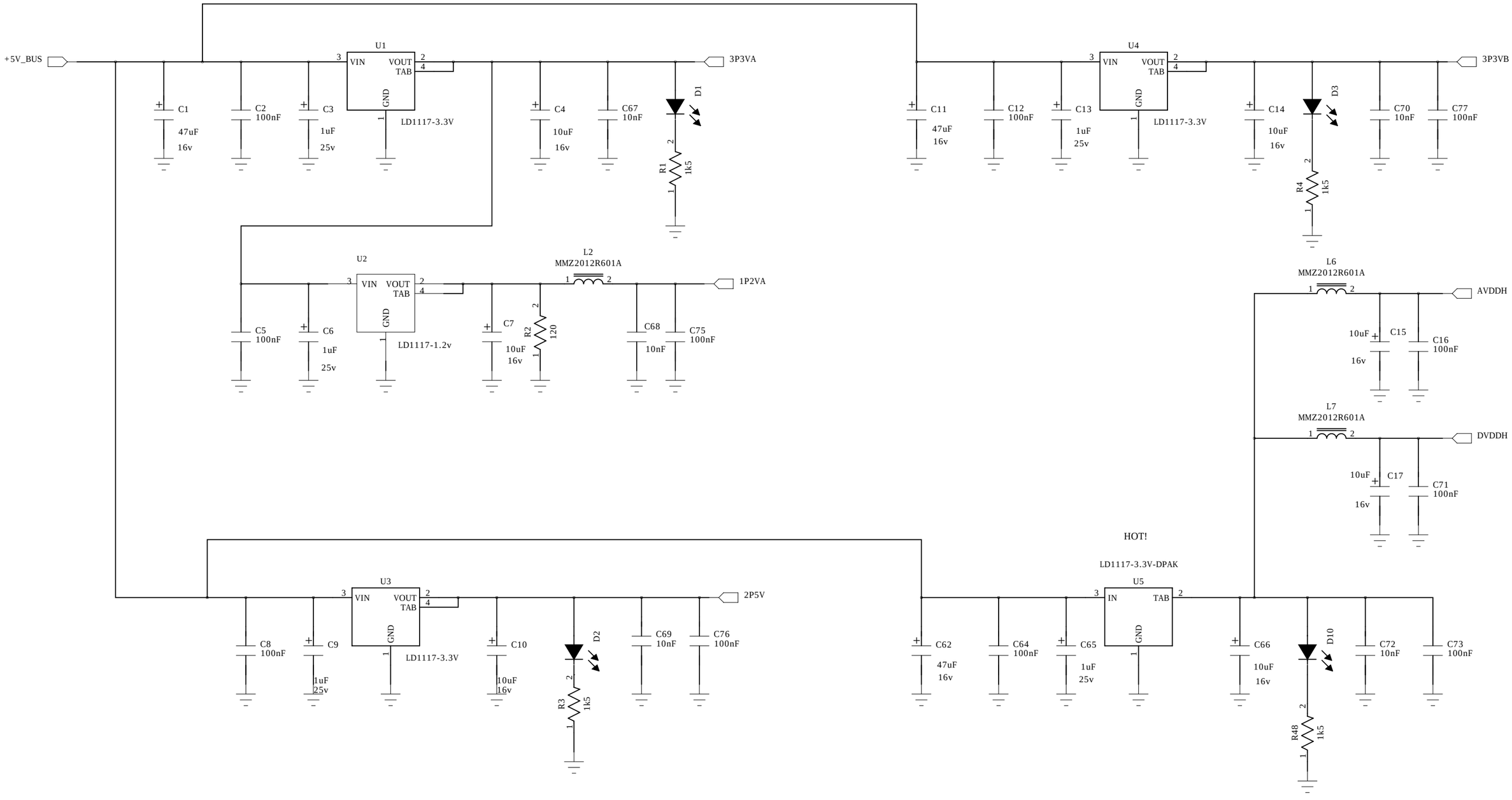

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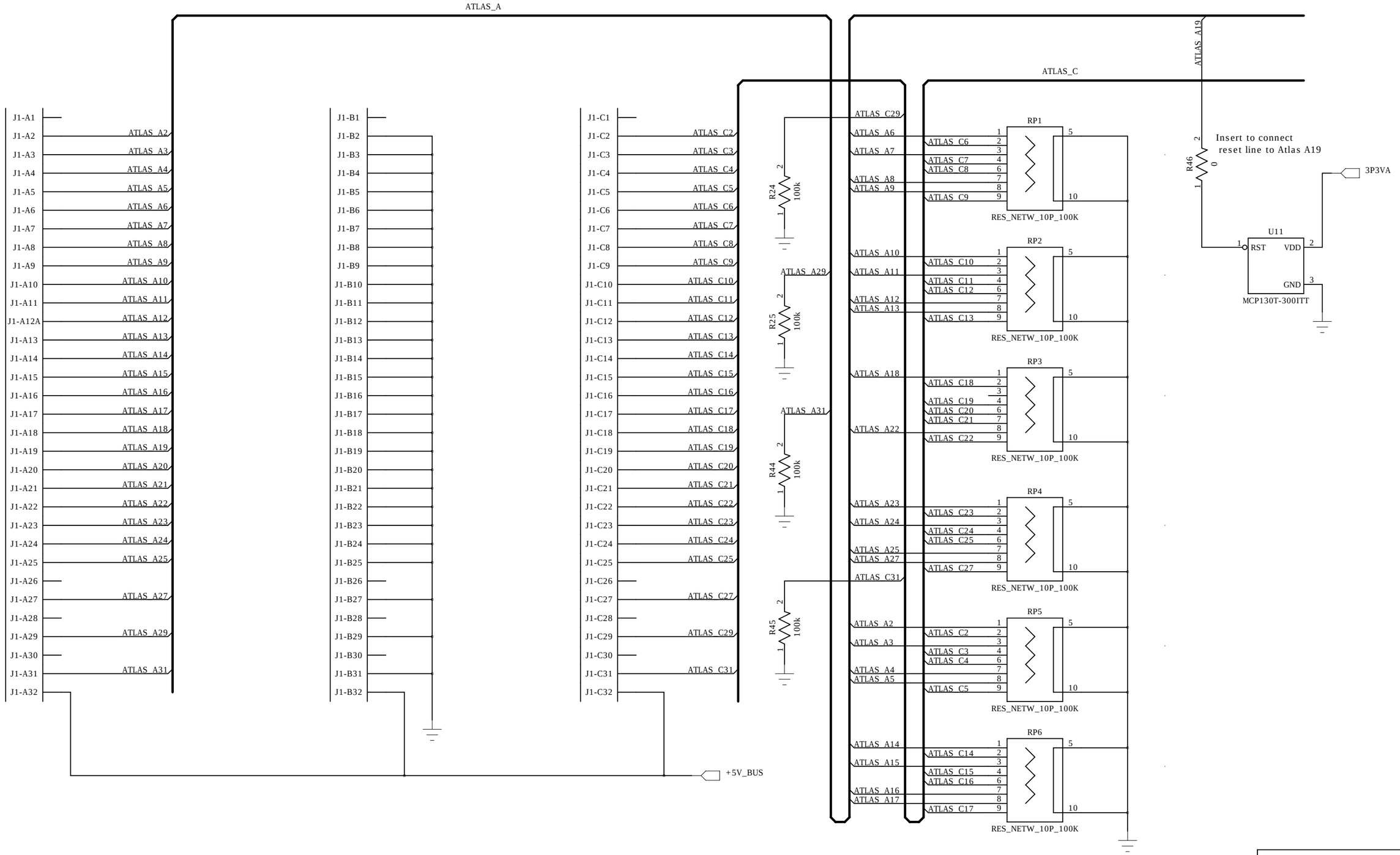

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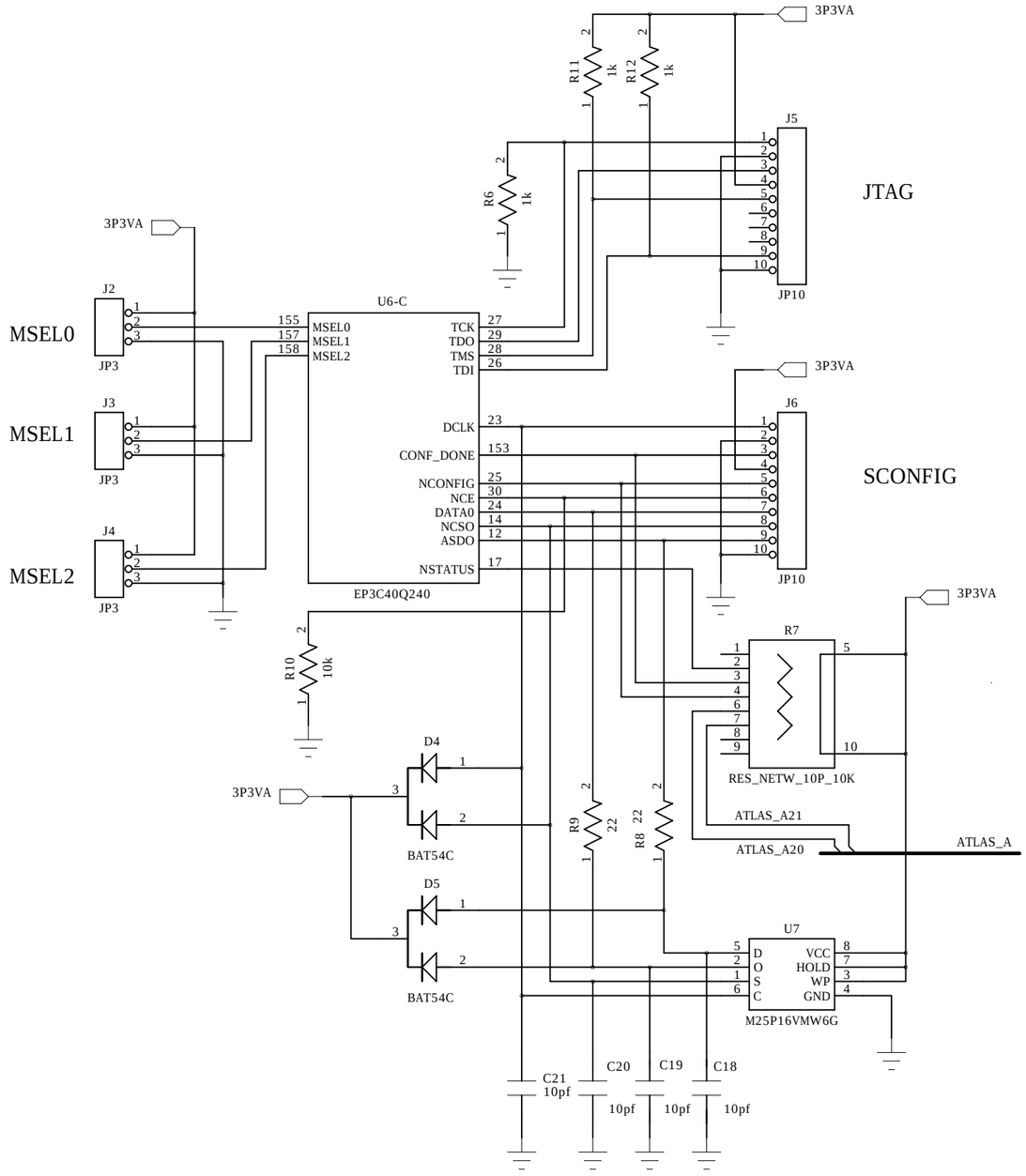
PS	1	0	0
FPP	1	1	0
JTAG	X	X	X



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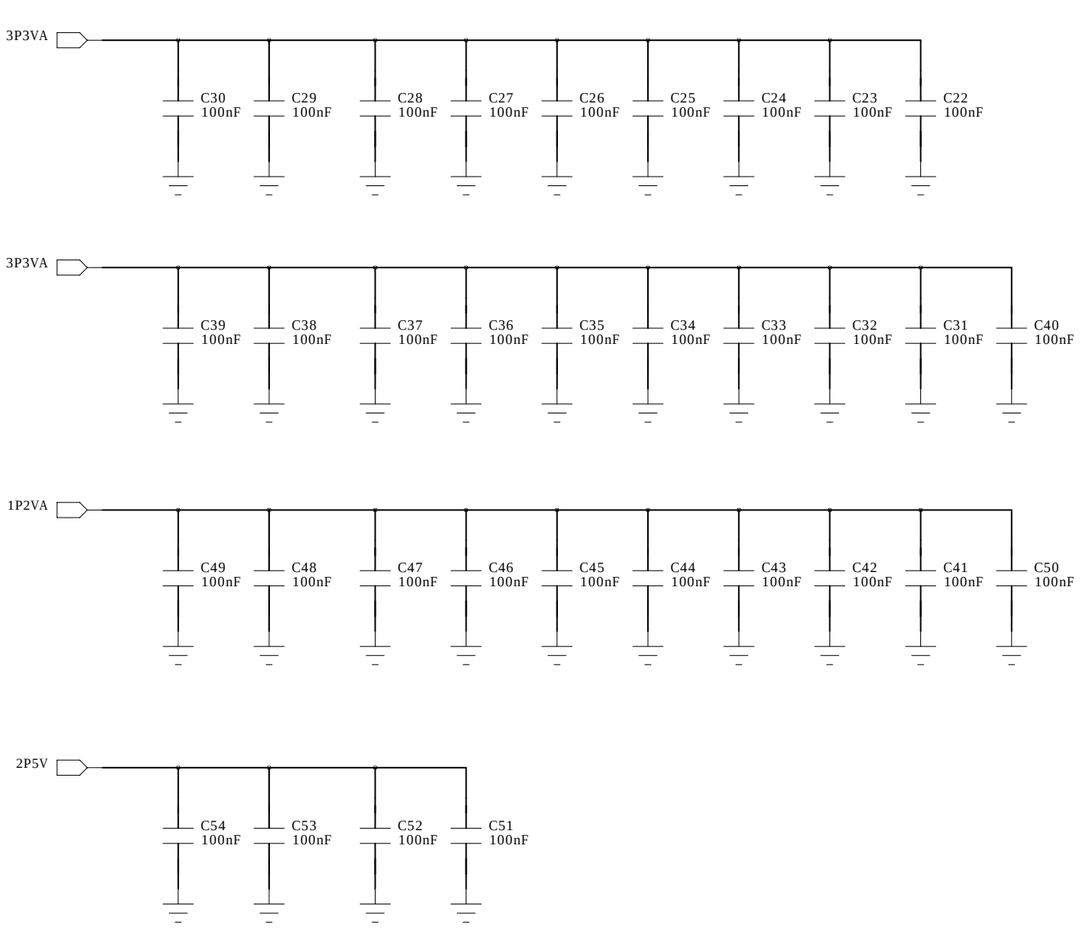

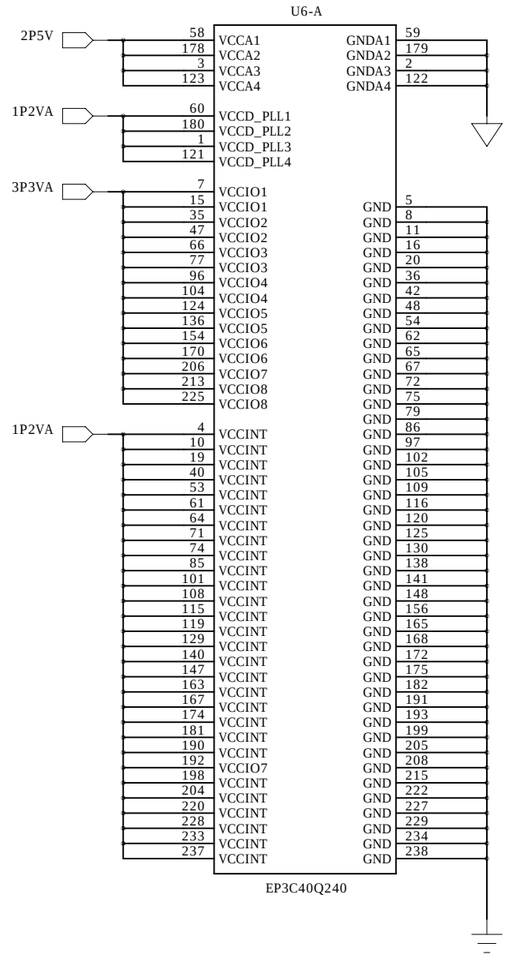

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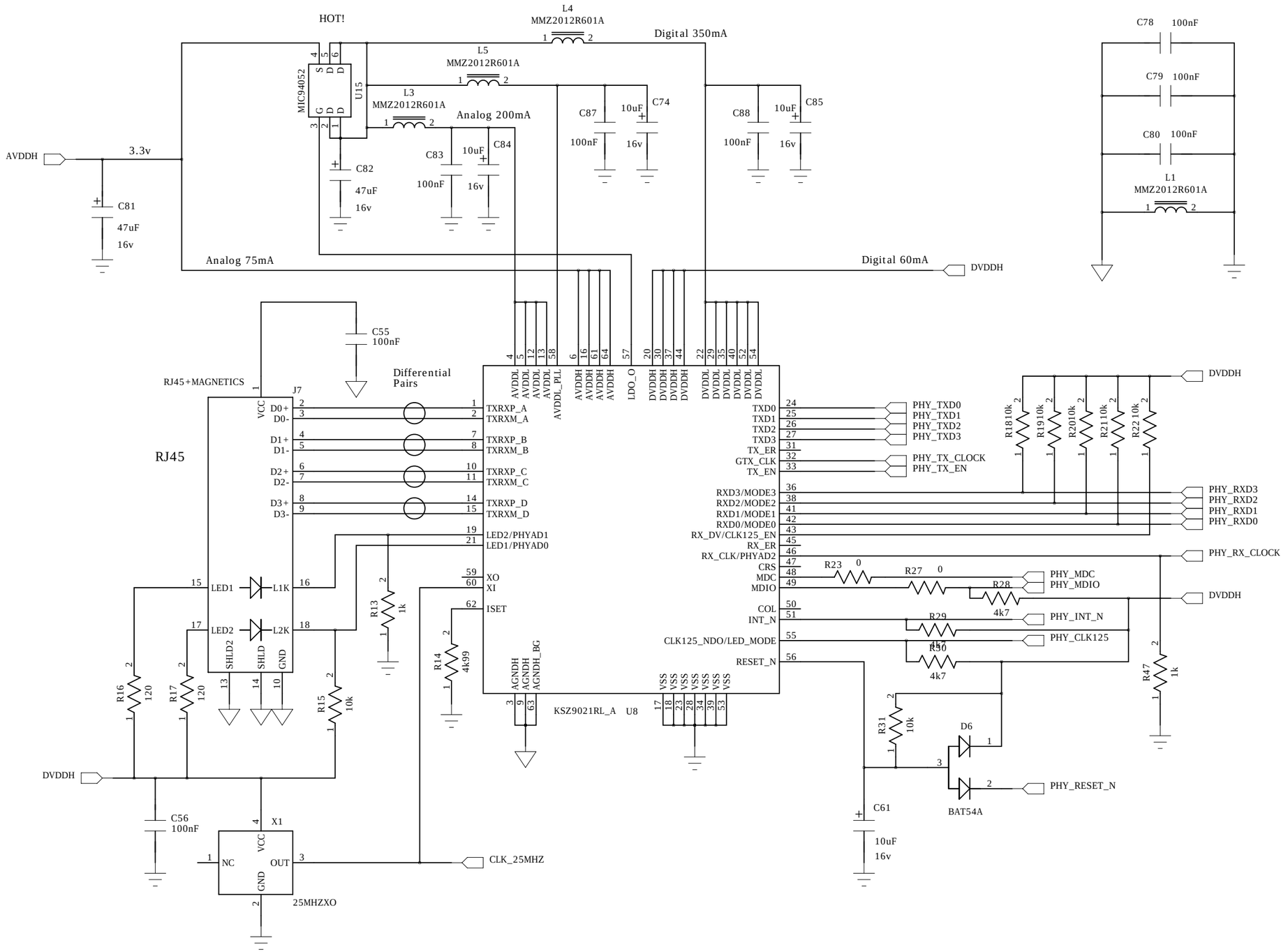

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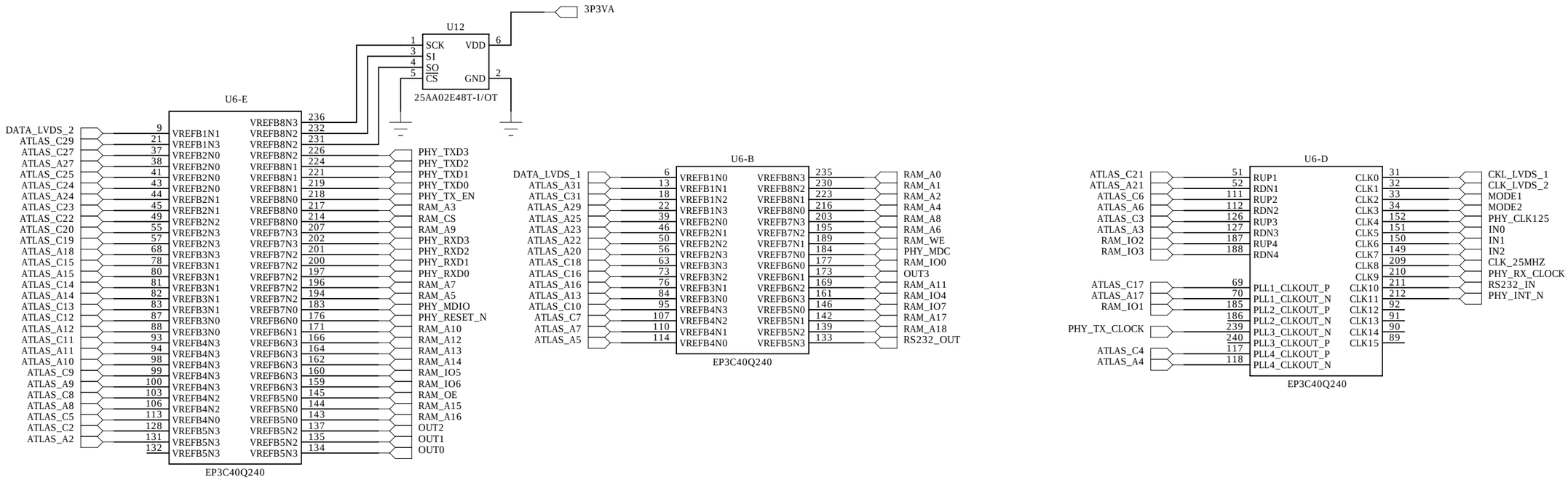
FPGA pin 1 top left

PHY pin 1 bottom right



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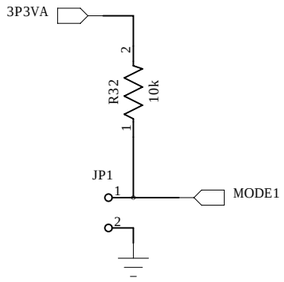

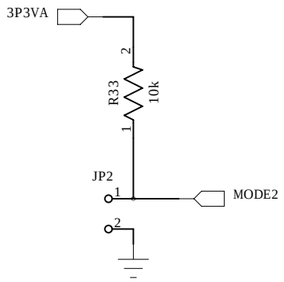

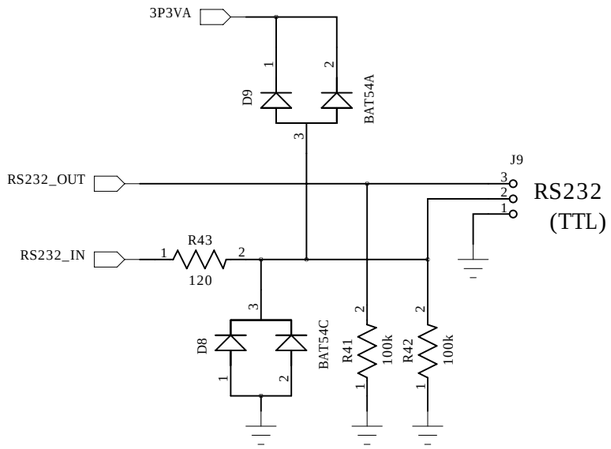

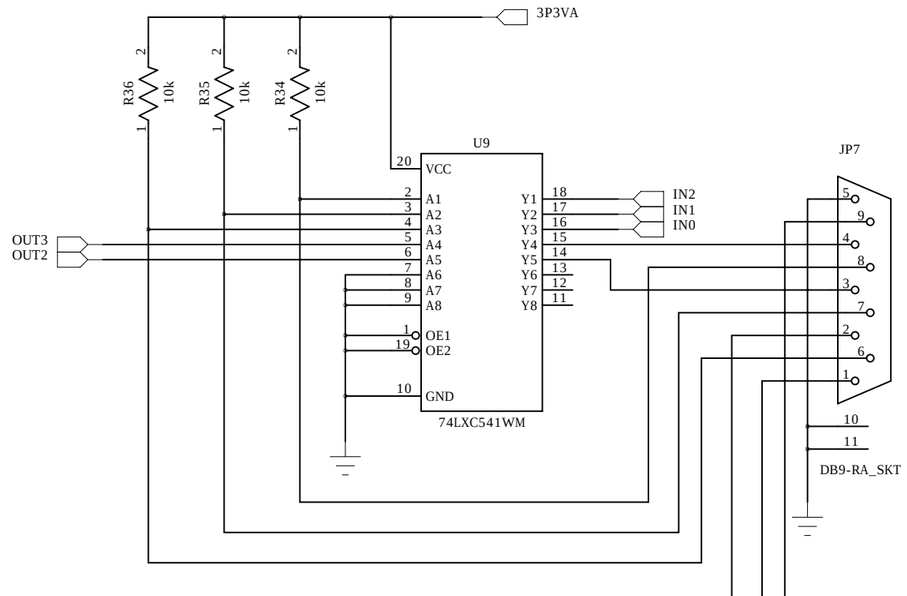

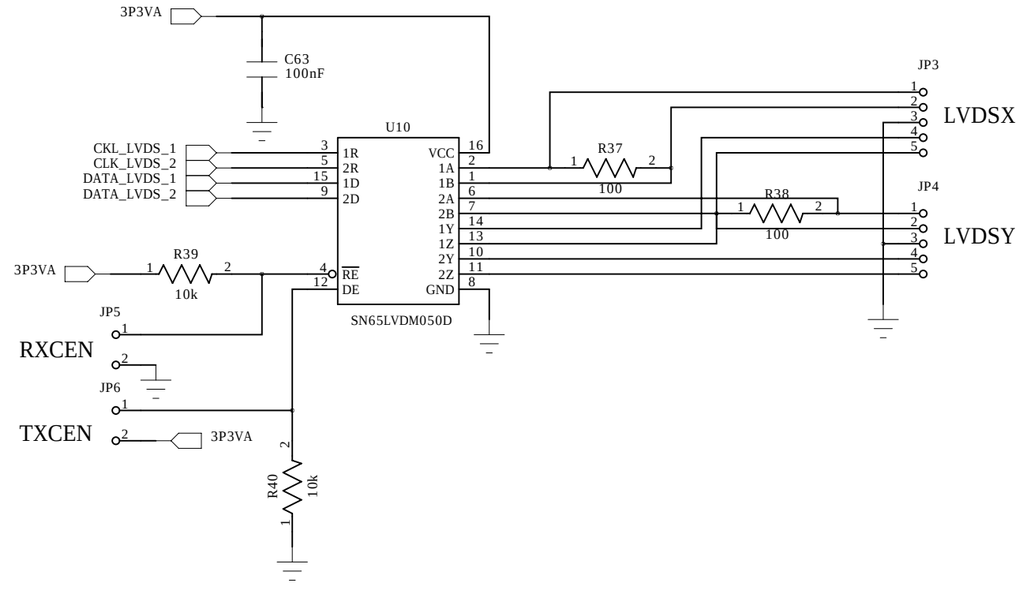

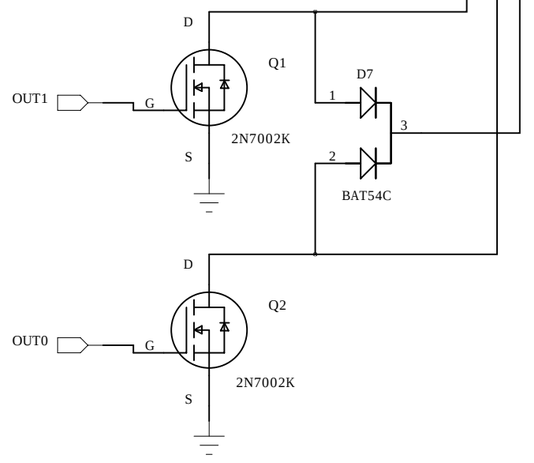

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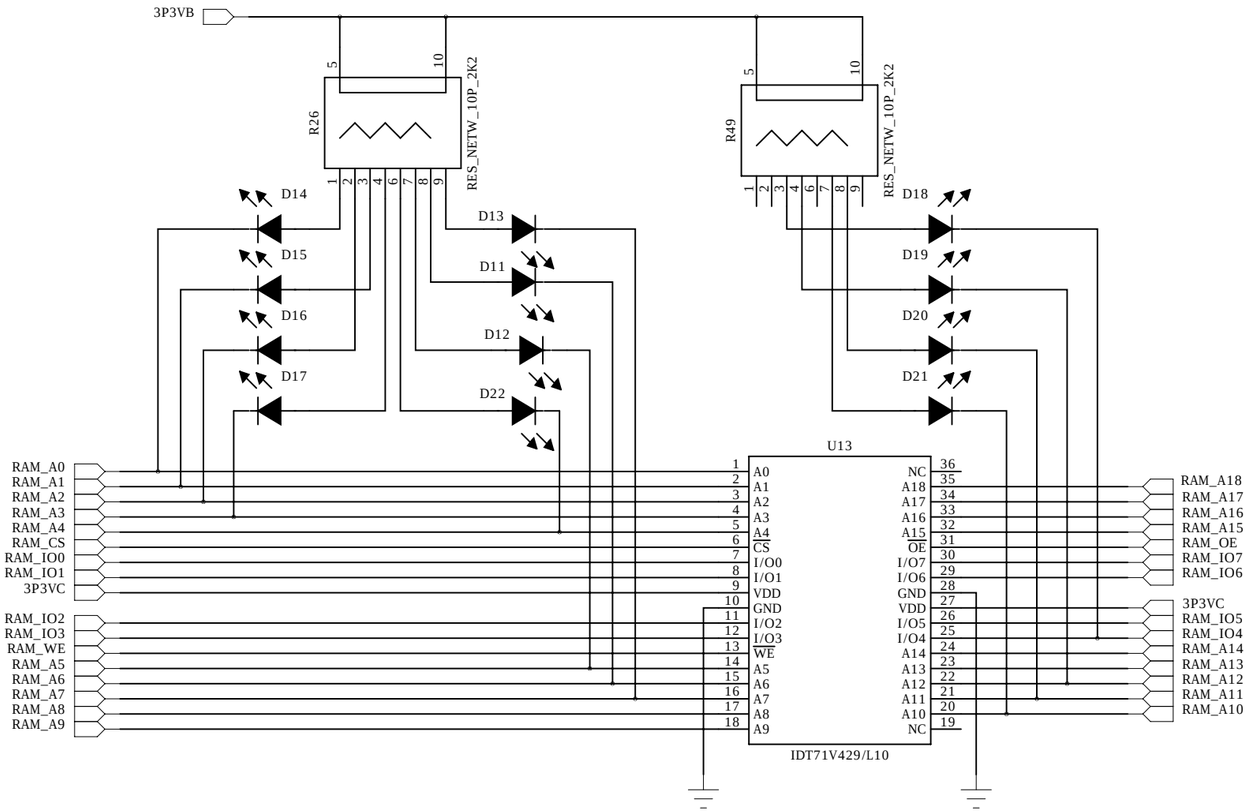

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